What is claimed is:

1. A stacked semiconductor module comprising:

a first upper switching element having:

a first semiconductor chip;

a first top electrode disposed at a top surface of the first semiconductor chip;

a first bottom electrode disposed at a bottom surface of the first semiconductor chip; and

a first control electrode configured to control conduction between the first top and first bottom electrodes;

a first wiring plate disposed beneath the first upper switching element, electrically connected to the first bottom electrode; and

a first lower switching element disposed beneath the wiring plate, having:

a second semiconductor chip;

a second top electrode disposed at a top surface of the second semiconductor chip, electrically connected to the first wiring plate;

a second bottom electrode disposed at a bottom surface of the second semiconductor chip,

a second control electrode configured to control conduction between the second top and second bottom electrodes;

2. The stacked semiconductor module of claim 1, further comprising:

a first power distribution plate electrically connected to the first top electrode; and

a second power distribution plate electrically connected to the second bottom electrode.

3. The stacked semiconductor module of claim 2, further comprising:

a second upper switching element having:

a third semiconductor chip;

a third top electrode disposed at a top surface of the third semiconductor chip, electrically connected to the first power distribution plate;

a third bottom electrode disposed at a bottom surface of the third semiconductor chip; and

a third control electrode configured to control conduction between the third top and third bottom electrodes;

a second wiring plate disposed beneath the second upper switching element, electrically connected to the third bottom electrode; and

a second lower switching element disposed beneath the second wiring plate, having:

a fourth semiconductor chip;

a fourth top electrode disposed at a top surface of the fourth semiconductor chip, electrically connected to the second wiring plate;

a fourth bottom electrode disposed at a bottom surface of the fourth semiconductor chip, electrically connected to the second power distribution plate; and

a fourth control electrode configured to control conduction between the fourth top and fourth bottom electrodes.

4. The stacked semiconductor module of claim 1, wherein the first power distribution plate comprises:

a first common beam;

a first upper branch diverged from the first common beam, electrically connected to the first top electrode; and

a first lower branch diverged from the first common beam, electrically connected to the first upper branch configured to extend beneath the second power distribution plate.

5. The stacked semiconductor module of claim 4, further comprising:

a second upper switching element disposed between the second power distribution plate and the first lower branch of the first power distribution plate having:

a third semiconductor chip;

a third top electrode disposed at a top surface of the third semiconductor chip,;

a third bottom electrode disposed at a bottom surface of the third semiconductor chip, electrically connected to the first lower branch of the first power distribution plate; and

a third control electrode configured to control conduction between the third top and third bottom electrodes;

a second wiring plate disposed above the second upper switching element, electrically connected to the third top electrode; and

a second lower switching element disposed between the second wiring plate and the second power distribution plate, having:

a fourth semiconductor chip;

a fourth top electrode disposed at a top surface of the fourth semiconductor chip, electrically connected to the second power distribution plate;

a fourth bottom electrode disposed at a bottom surface of the fourth semiconductor chip, electrically connected to the second wiring plate; and

a fourth control electrode configured to control conduction between the fourth top and fourth bottom electrodes.

6. The stacked semiconductor module of claim 5, wherein the second power distribution plate comprises:

a second common beam running in parallel and adjacently with the first common beam;

a second upper branch diverged from the second common beam, electrically connected to the fourth top electrode; and

a second lower branch diverged from the second common beam, electrically connected to the second upper branch configured to extend beneath the first lower branch of the first power distribution plate.

7. The stacked semiconductor module of claim 2, further comprising:

an upper diode having:

a first diode chip;

a first cathode electrode disposed at a top surface of the first diode chip, electrically connected to the first power distribution plate; and

a first anode electrode disposed at a bottom surface of the first diode chip, electrically connected to the first wiring plate; and

a lower diode disposed beneath the first wiring plate, having:

a second diode chip;

a second cathode electrode disposed at a top surface of the second diode chip, electrically connected to the first wiring plate; and

a second anode electrode disposed at a bottom surface of the second diode chip, electrically connected to the second power distribution plate.

8. The stacked semiconductor module of claim 1, wherein the first control electrode is disposed at the bottom surface of the first semiconductor chip.

9. The stacked semiconductor module of claim 8, further comprising a first control electrode wiring disposed in a recessed region of the first wiring plate, electrically connected to the first control electrode.

10. The stacked semiconductor module of claim 1, wherein the first control electrode is disposed at the top surface of the first semiconductor chip.

11. The stacked semiconductor module of claim 10, further comprising a first control electrode wiring disposed in a recessed region of the first power distribution plate, electrically connected to the first control electrode.

12. The stacked semiconductor module of claim 1, wherein the second control electrode is disposed at the bottom surface of the second semiconductor chip.

13. The stacked semiconductor module of claim 12, further comprising a second control electrode wiring disposed in a

recessed region of the second power distribution plate, electrically connected to the second control electrode.

14. The stacked semiconductor module of claim 2, further comprising:

a first upper thermal buffering layer disposed between the first power distribution plate and the first top electrode;

a first lower thermal buffering layer disposed between the first bottom electrode and the first wiring plate;

a second upper thermal buffering layer disposed between the first wiring plate and the second top electrode;

a second lower thermal buffering layer disposed between the second bottom electrode and the second power distribution plate and first top electrode,

wherein the first upper, the first lower, the second upper and second lower thermal buffering layer are respectively made of material having a lower coefficient of thermal expansion than the material implementing the first power distribution plate, the first wiring plate, or the second power distribution plate.

15. The stacked semiconductor module of claim 14, further comprising a mechanism configured to press-contact vertically the laminated structure of the first power distribution plate, the first upper thermal buffering layer, the first upper switching element, the first lower thermal buffering layer, the first wiring plate, the second upper thermal buffering layer, the first lower

switching element, the a second lower thermal buffering layer and the second power distribution plate.

16. The stacked semiconductor module of claim 14, further comprising:

an upper insulation layer having a window installing the first upper thermal buffering layer, being disposed between the first power distribution plate and the first upper switching element; and

a lower insulation layer having a window installing the first lower thermal buffering layer, being disposed between the first upper switching element and the first wiring plate.

17. The stacked semiconductor module of claim 16, wherein the first upper switching element is positioned by recesses formed at a top surface of the upper insulation layer and at a bottom surface of the lower insulation layer, respectively.

18. The stacked semiconductor module of claim 16, wherein the first power distribution plate has a protrusion protruding toward the first upper switching element so as to mate with a top surface of the first upper thermal buffering layer in a flat plane, and the first wiring plate has a protrusion protruding toward the first upper switching element so as to mate with a bottom surface of the first lower thermal buffering layer in a flat plane.

19. A method for assembling a stacked semiconductor module, comprising:

forming a lower insulation layer having a window on a second power distribution plate;

mounting a lower switching element on the second power distribution plate aligned by the window of the lower insulation layer;

stacking a wiring plate on the lower switching element;

forming an upper insulation layer having a window on the wiring plate;

mounting an upper switching element on the wiring plate aligned by the window of the upper insulation layer;

stacking a first power distribution plate on the upper switching element.

20. A stacked semiconductor module comprising:

an upper switching means for controlling conduction between first top and first bottom electrodes;

a lower switching means for controlling conduction between second top and second bottom electrodes;

a wiring means for electrically connecting both to the first bottom electrode and second top electrode; and

a means for press-contact vertically a laminated structure comprising the upper switching means, the lower switching means and the wiring means.